

## bq4050 CEDV Gas Gauge and Protection Solution for 1-Series to 4-Series Cell Li-Ion Battery Packs

### 1 Features

- High-Side Protection N-CH FET Drive Allows Serial Bus Communication During Fault Conditions
- Cell Balancing with Internal Bypass Optimizes Battery Health
- Diagnostic Lifetime Data Monitor and Black Box Recorder for Failure Analysis
- Full Array of Programmable Protection Features: Voltage, Current, Temperature
- JEITA Charge Algorithms Support Smart Charging
- Analog Front End with Two Independent ADCs
  - Simultaneous Current and Voltage Sampling
  - High-Accuracy Coulomb Counter with Input Offset Error < 1  $\mu$ V (Typical)
- Supports Battery Trip Point (BTP) Function for Windows® Integration
- LED Display for State of Charge and Battery Status Indication
- 100-KHz SMBus v1.1 Communications Interface for Programming and Data Access with Alternate 400-KHz Mode
- SHA-1 Authentication Responder for Increased Battery Pack Security
- Compact 32-pin VQFN Package (RSM)

### 2 Applications

- Notebook/Netbook PCs
- Medical and Test Equipment
- Portable Instrumentation

### 3 Description

The Texas Instruments bq4050 device, incorporating Compensated End-of-Discharge Voltage (CEDV) technology, is a highly integrated, accurate, 1-series to 4-series cell gas gauge and protection solution, enabling autonomous charger control and cell balancing.

The bq4050 device provides a fully integrated pack-based solution with a flash programmable custom reduced instruction-set CPU (RISC), safety protection, and authentication for Li-Ion and Li-Polymer battery packs.

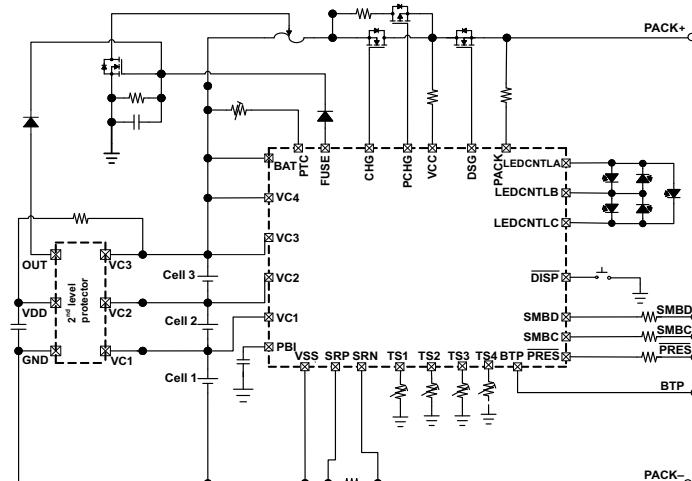
The bq4050 gas gauge communicates via an SMBus-compatible interface and combines an ultra-low power, high-speed TI bqBMP processor, high-accuracy analog measurement capabilities, integrated flash memory, an array of peripheral and communication ports, an N-CH FET drive, and a SHA-1 Authentication transform responder into a complete, high-performance battery management solution.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq4050	VQFN (32)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCT PREVIEW Information. Product in design phase of development. Subject to change or discontinuance without notice.

## 4 Device and Documentation Support

### 4.1 Documentation Support

#### 4.1.1 Related Documentation

For related documentation, see the *bq4050 Technical Reference Manual (SLUUAQ3)*.

### 4.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 4.3 Trademarks

E2E is a trademark of Texas Instruments.

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All other trademarks are the property of their respective owners.

### 4.4 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 4.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ4050RSMR	PREVIEW	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ4050	
BQ4050RSMT	PREVIEW	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ4050	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## PACKAGE OPTION ADDENDUM

18-Feb-2016

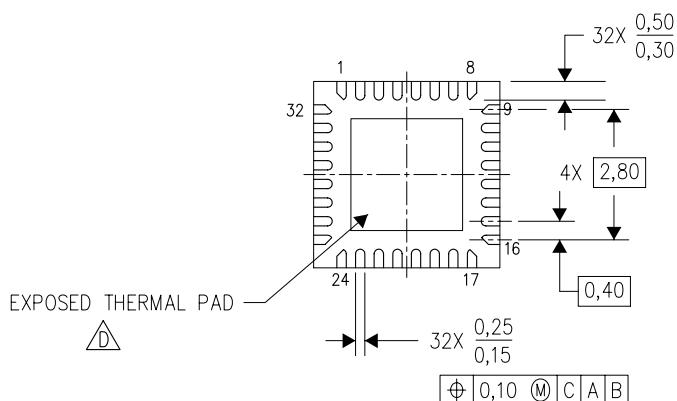
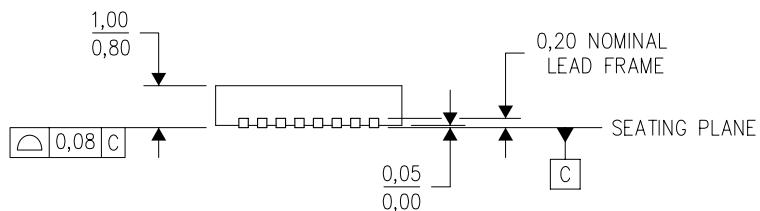
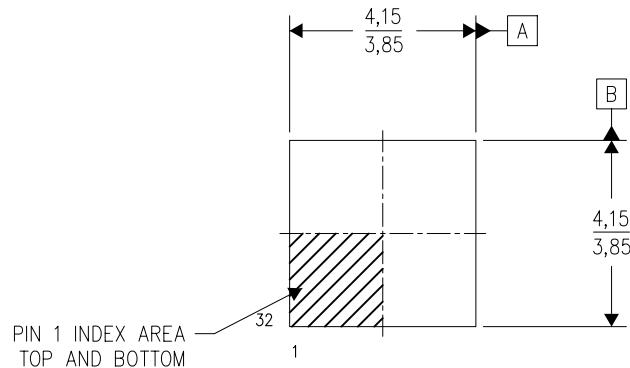
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## MECHANICAL DATA

RSM (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4207560/B 03/10

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- QFN (Quad Flatpack No-Lead) Package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

RSM (S-PVQFN-N32)

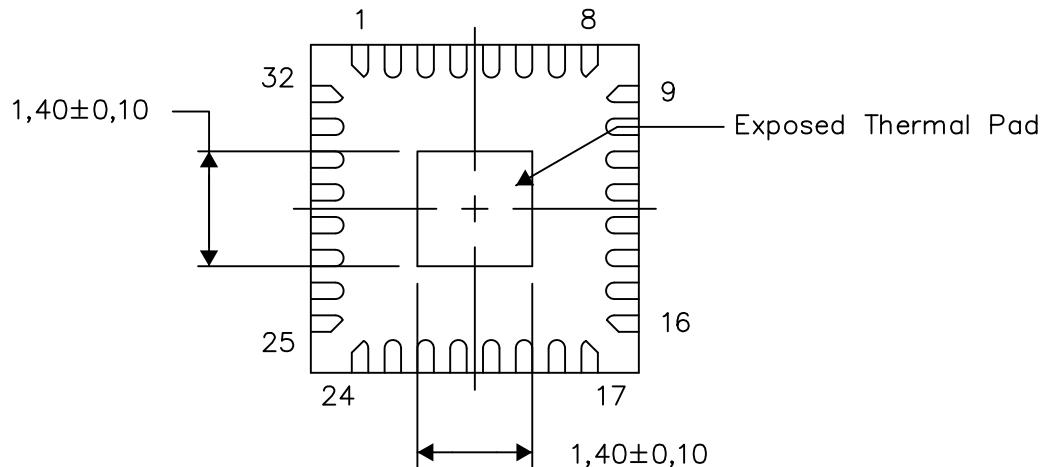
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

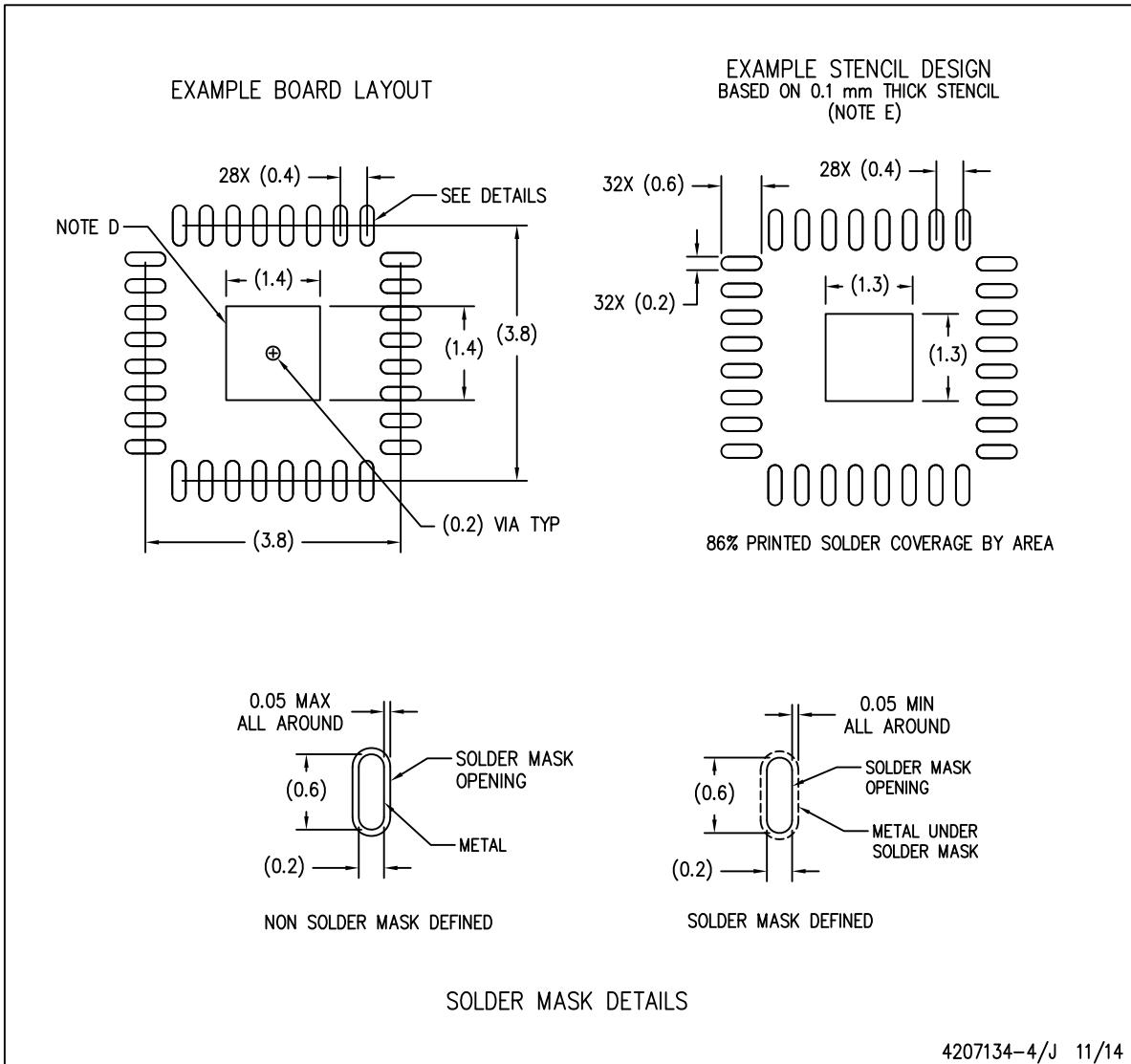
Exposed Thermal Pad Dimensions

4207868-3/1 07/14

NOTE: All linear dimensions are in millimeters

RSM (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4207134-4/J 11/14

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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